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TITLE: METHOD OF MAKING UNIFORM OXIDE LAYER

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METHOD OF MAKING UNIFORM OXIDE LAYER

BACKGROUND

The present invention relates to methods of forming oxides layers in semiconductor structures.

A widely used isolation technique in semiconductor structures is silicon trench isolation (STI), shown in Figure 5. A field oxide **4** narrows into an oxide layer **10** on a silicon substrate **2**. Figures 1-4 illustrate the steps used to prepare the structure shown in Figure 5. Thermal oxidizing forms an oxide layer (SiO_2) **10** on the silicon substrate **2**, followed by depositing a silicon nitride (Si_3N_4) layer (isolation nitride) **6** using low pressure chemical vapor deposition (LPCVD) to form the structure shown in Figure 1. Next, a photoresist layer **12** is applied, and patterned using a mask. Etching of those portions of the silicon nitride layer, thermal oxide and silicon substrate not covered by the photoresist layer, in a single operation, opens a trench **14**, giving the structure shown in Figure 2.

The photoresist layer is then stripped, and the substrate is cleaned. An oxide layer **16** is then deposited into the trench and across the surface of the structure by chemical vapor deposition (CVD), producing the structure shown in Figure 3. Chemical-mechanical polishing (CMP) planarizes the surface, leaving the oxide layer **16** only in the trench, as shown in Figure 4. The silicon nitride layer is removed, to produce the structure shown in Figure 5. Typically, further processing will include ion implantation through the oxide layer **10**, using it as a screen oxide, to form source/drain regions, and then removal of the screen oxide followed by growth of a gate oxide layer on the silicon substrate. At this point, completion of a semiconductor device, by the formation of gates, contacts, metallization, etc., may be carried out, and the semiconductor device may then be incorporated into an electronic device.

During CMP to planarize the surface of the structure, the center to edge uniformity across the wafer is very poor. Consequently, the thickness of the silicon nitride layer varies across the wafer. The silicon nitride layer is typically removed by etching with a phosphoric acid etch. Since the etch is

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continued for a time sufficient to remove the nitride layer, over etching is necessary to ensure that all of the silicon nitride is removed. Furthermore, during LPCVD silicon nitride is deposited on both the front and back sides of the wafer; over etching is necessary to ensure remove of the silicon nitride on the back side of the wafer, to avoid interference with the stepper.

The silicon nitride/silicon oxide selectivity of the silicon nitride etching changes as the bath of phosphoric acid is used. A fresh phosphoric acid bath will etch silicon oxide slowly, and as the bath is used, the rate of etching of silicon oxide will slow down, stop and eventually begin to deposit oxide. The thickness of the oxide layer (typically used as a screen oxide during ion implantation) is usually 125 Å when initially formed, will have a variable thickness at the end of this process, depending on the age of the phosphoric acid bath used during the etching of the silicon nitride layer, and the amount of over etching. The variable thickness of the screen oxide will affect the formation of the source/drain regions, leading to inconsistent threshold voltages (Vt) for the transistors formed on the wafer.

BRIEF SUMMARY

In a first aspect, the present invention is a method of forming a semiconductor structure, including forming an isolation region in a semiconductor substrate. A first oxide layer is on the substrate, a first sacrificial layer is on the first oxide layer, and a first nitride layer is on the first sacrificial layer.

In a second aspect, the present invention is a method of forming a semiconductor structure, including removing a first nitride layer and a first sacrificial layer. A first oxide layer is on a substrate, the first sacrificial layer is on the first oxide layer, and the first nitride layer is on the first sacrificial layer.

In a third aspect, the present invention is a method of forming a semiconductor device from either of these structures.

In a fourth aspect, the present invention is a method of forming an electronic device from this semiconductor device.

The term "oxide" refers to a metal oxide conventionally used to isolate electrically active structures in an integrated circuit from each other, typically an oxide of silicon and/or aluminum (e.g., SiO_2 or Al_2O_3, which may be conventionally doped with fluorine, boron, phosphorous or a mixture thereof; preferably SiO_2 or SiO_2 conventionally doped with 1-12 wt% of phosphorous and 0-8 wt% of boron).

BRIEF DESCRIPTION OF THE DRAWINGS

Various other objects, features and attendant advantages of the present invention will be more fully appreciated as the same becomes better understood from the following detailed description when considered in connection with the accompanying drawings in which like reference characters designate like or corresponding parts throughout the several views and wherein:

Figures 1-4 illustrate the formation of a silicon trench isolation region;

Figure 5 shown a silicon trench isolation region;

Figures 6-11 illustrate an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention includes a first sacrificial layer on the screen oxide layer, and optionally, a second sacrificial layer between the first sacrificial layer, and the screen oxide layer. The first sacrificial layer acts as a sacrificial layer during the silicon nitride etch, providing a stopping point for the etch, but any damage to this layer will be irrelevant since it is subsequently remove. This layer is then removed, as well as the optional second sacrificial layer. Since the sacrificial layer (or layers) is relatively thin, only a small amount of damage is possible to the screen oxide layer, ensuring a more consistent thickness and therefore a consistent Vt for the semiconductor device.

The first sacrificial layer may be made from any material that will act as an etch stop for silicon nitride. For example, the first sacrificial layer may include silicon (such as polycrystalline silicon), tungsten, tungsten silicide, or

titanium nitride. The second sacrificial layer may be made from any material that can be selectively etched over silicon oxide. For example, the second sacrificial layer may include silicon (such as polycrystalline silicon), tungsten, tungsten silicide, or titanium nitride. If the second sacrificial layer is not present, then the first sacrificial layer must also be able to be selectively etched over silicon oxide. In a preferred embodiment, both the first and second sacrificial layers are present. More preferably, the first sacrificial layer includes silicon oxide (SiO_2), and the second sacrificial layer comprises silicon nitride (Si_3N_4).

Preferably, the sacrificial layer (or layers) is thinner than the isolation nitride layer. More preferably, the first sacrificial layer has a thickness of 5 to 1000 Å, more preferably 10 to 250 Å, most preferably 20 to 100 Å, for example 50 Å. More preferably, the second sacrificial layer has a thickness of 5 to 1000 Å, more preferably 10 to 500 Å, most preferably 30 to 200 Å, for example 100 Å. The screen oxide preferably has a thickness of 5 to 1000 Å, more preferably 10 to 500 Å, most preferably 30 to 200 Å, for example 125 Å. The isolation nitride layer preferably has a thickness of 100 to 20,000 Å, more preferably 200 to 10,000 Å, most preferably 500 to 4000 Å, for example 1950 Å.

An embodiment of the present invention is illustrated in Figures 6-11. First, thermal oxidation of a silicon substrate forms a screen oxide **110**, followed by LPCVD of a second sacrificial layer **120**, containing silicon nitride. CVD of a first sacrificial layer **118**, containing silicon oxide, onto the second sacrificial layer **120** is then followed by LPCVD of an isolation nitride layer **106**. This forms the structure shown in Figure 6.

A photoresist layer **112** is applied, and patterned. The isolation nitride layer, both sacrificial layers, the screen oxide layer, and the substrate, are etched, to form a trench **114**. The resulting structure is illustrated in Figure 7. The field isolation dielectric **116**, preferably an oxide, is applied across the substrate, filling the trench, to form the structure shown in Figure 8.

CMP is used to bring the surface of the field isolation dielectric **116** down to the level of the isolation nitride **106**, as illustrated in Figure 9. Then

the isolation nitride **106** is removed, by etching with phosphoric acid. Over etching may be used to ensure removal of all of the isolation nitride across the substrate, as well as any nitride present on the back of substrate. An etchant, such as hydrofluoric acid, may then be used to remove the first sacrificial layer **118**, to produce the structure shown in Figure 10.

The second sacrificial layer **120**, is removed, by etching with phosphoric acid. Preferably, this layer is much thinner than the isolation nitride layer, and has not been subjected to CMP, and therefore no over etching, or very little over etching, is necessary in order to completely remove this layer. The structure of Figure 11 is then formed, with a screen oxide **110** have a very consistent thickness; the thickness will be very close to the thickness with which it was originally formed. Preferably, the thickness will deviate by no more than 30 Å (+/- 30 Å), more preferably by no more than 20 Å (+/- 20 Å), most preferably by no more than 10 Å (+/- 10 Å), from the thickness with which it was originally formed. Preferably, the thickness will deviate by no more than 25%, more preferably by no more than 15%, most preferably by no more than 10%, from the thickness with which it was originally formed.

In the case where only a single sacrificial layer is present, such as a polycrystalline silicon layer, the structure shown in Figure 11 would be formed directly after etching the isolation nitride layer and the sacrificial layer. The single sacrificial layer would protect the underlying screen oxide layer from damage during the etching of the isolation nitride layer.

The present invention may be used in conjunction with any method of forming an isolation region, as long as an isolation nitride is used in the process. Such methods may be modified to use the present invention by including a sacrificial layer between the substrate and the isolation nitride layer. Preferably, two sacrificial layers are used, more preferably, the first sacrificial layer is an oxide layer and the second sacrificial layer is a nitride layer between the substrate and the first sacrificial layer. Examples of other methods of forming isolation regions include those described in application Serial Nos. 09/505,737 and 08/885,046.

The individual processing steps, including etching and deposition steps, for use in the present invention are well known to those of ordinary skill in the art, and are also described in Encyclopedia of Chemical Technology, Kirk-Othmer, Volume 14, pp. 677-709 (1995); Semiconductor Device Fundamentals, Robert F. Pierret, Addison-Wesley, 1996; Wolf, Silicon Processing for the VLSI Era, Lattice Press, 1986, 1990, 1995 (vols 1-3, respectively), and Microchip Fabrication 3rd. edition, Peter Van Zant, McGraw-Hill, 1997. The isolation nitride, as well as the first or second sacrificial layers when they include nitride, may be formed by CVD, preferably LPCVD or plasma enhanced CVD (PECVD).

When nitride, oxide and/or sacrificial layers are removed, they are selectively etched, and the layer they are on acts as the etch stop layer. Preferably, the etch selectivity (i.e., the ratio of (a) the rate of dielectric etching to (b) the rate of etch stop material etching) is at least 2:1, preferably at least 3:1, more preferably at least 5:1 and even more preferably at least 10:1. In the case of etching silicon oxide using silicon nitride as the etch-stop layer, an etching solution of one part HF(49%) in one part deionized water will give a selectivity of greater than 1:300.

The substrate may typically be a semiconductor material conventionally known by those of ordinary skill in the art. Examples include silicon, gallium arsenide, germanium, gallium nitride, aluminum phosphide, and alloys such as $Si_{1-x}Ge_x$ and $Al_xGa_{1-x}As$, where 0 x 1. Many others are known, such as those listed in Semiconductor Device Fundamentals, on page 4, Table 1.1 (Robert F. Pierret, Addison-Wesley, 1996). Preferably, the semiconductor substrate is silicon, which may be doped or undoped.

The structures of the present invention may be incorporated into a semiconductor device such as an integrated circuit, for example a memory cell such as an SRAM, a DRAM, an EPROM, an EEPROM etc.; a programmable logic device; a data communications device; a clock generation device; etc. Furthermore, any of these semiconductor devices may be incorporated in an electronic device, for example a computer, an airplane or an automobile.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

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